ANALOG DEVICES

10 MHz Bandwidth, 640 MSPS
Dual Continuous Time Sigma-Delta Modulator

AD9267

FEATURES

SNR: 83 dB (85 dBFS) to 10 MHz input
SFDR: −88 dBc to 10 MHz input
Noise figure: 15 dB
Input impedance: 1 kΩ
Power: 416 mW
10 MHz real or 20 MHz complex bandwidth
1.8 V analog supply operation
On-chip PLL clock multiplier
On-chip voltage reference
Twos complement data format
640 MSPS, 4-bit LVDS data output
Serial control interface (SPI)

APPLICATIONS

Baseband quadrature receivers: CDMA2000, W-CDMA,
    multicarrier GSM/EDGE, 802.16x, and LTE
Quadrature sampling instrumentation

GENERAL DESCRIPTION

The AD9267 is a dual continuous time (CT) sigma-delta (Σ-Δ) modulator with −88 dBc of dynamic range over 10 MHz real or 20 MHz complex bandwidth. The combination of high dynamic range, wide bandwidth, and characteristics unique to the continuous time Σ-Δ modulator architecture makes the AD9267 an ideal solution for wireless communication systems.

The AD9267 has a resistive input impedance that significantly relaxes the requirements of the driver amplifier. In addition, a 32× oversampled fifth-order continuous time loop filter attenuates out-of-band signals and aliases, reducing the need for external filters at the input. The low noise figure of 15 dB relaxes the linearity requirements of the front-end signal chain components, and the high dynamic range reduces the need for an automatic gain control (AGC) loop.

A differential input clock controls all internal conversion cycles. An external clock input or the integrated integer-N PLL provides the 640 MHz internal clock needed for the oversampled continuous time Σ-Δ modulator. The digital output data is presented as 4-bit, LVDS at 640 MSPS in twos complement format. A data clock output (DCO) is provided to ensure proper latch timing with receiving logic. Additional digital signal processing may be required on the 4-bit modulator output to remove the out-of-band noise and to reduce the sample rate.
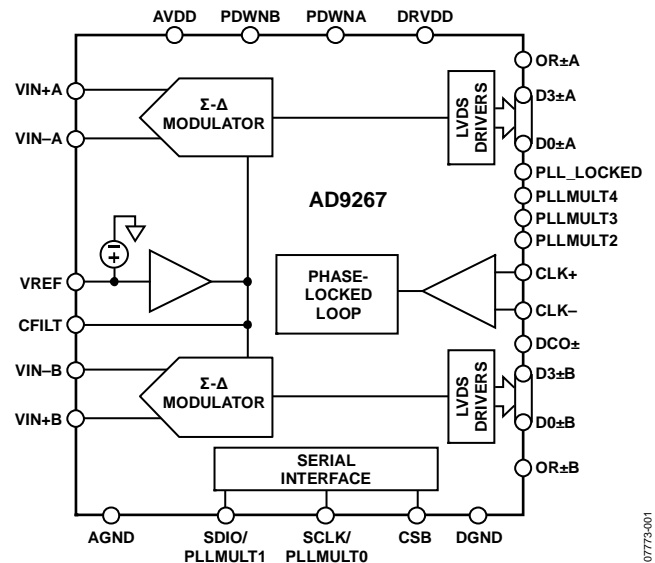
FUNCTIONAL BLOCK DIAGRAM

Figure 1.

The AD9267 operates on a 1.8 V power supply, consuming 416 mW. The AD9267 is available in a 64-lead LFCSP and is specified over the industrial temperature range (−40°C to +85°C).

PRODUCT HIGHLIGHTS

1. Continuous time Σ-Δ architecture efficiently achieves high dynamic range and wide bandwidth.
2. Passive input structure reduces or eliminates the requirements for a driver amplifier.
3. An oversampling ratio of 32× and high order loop filter provide excellent alias rejection, reducing or eliminating the need for antialiasing filters.
4. Operates from a single 1.8 V power supply.
5. A standard serial port interface (SPI) supports various product features and functions.
6. Features a low pin count, high speed LVDS interface with data output clock.

AD9267* PRODUCT PAGE QUICK LINKS

Last Content Update: 09/27/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD9267 Evaluation Board

DOCUMENTATION

Application Notes

- AN-1142: Techniques for High Speed ADC PCB Layout
- AN-282: Fundamentals of Sampled Data Systems
- AN-283: Sigma-Delta ADCs and DACs
- AN-807: Multicarrier WCDMA Feasibility
- AN-808: Multicarrier CDMA2000 Feasibility
- AN-812: MicroController-Based Serial Port Interface (SPI) Boot Circuit
- AN-835: Understanding High Speed ADC Testing and Evaluation
- AN-878: High Speed ADC SPI Control Software
- AN-905: Visual Analog Converter Evaluation Tool Version 1.0 User Manual

Data Sheet

- AD9267: 10 MHz Bandwidth, 640 MSPS Dual Continuous Time Sigma-Delta Modulator Preliminary Data Sheet

User Guides

- UG-093: Evaluation Board User Guide for the Dual, Continuous Time Sigma-Delta Modulator

REFERENCE MATERIALS

Technical Articles

- MS-2210: Designing Power Supplies for High Speed ADC
- Understanding Continuous-Time, Discrete-Time Sigma-Delta ADCs And Nyquist ADCs

DESIGN RESOURCES

- AD9267 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD9267 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

AD9267

TABLE OF CONTENTS

REVISION HISTORY

7/09—Revision 0: Initial Version

SPECIFICATIONS

DC SPECIFICATIONS

All power supplies set to 1.8 V, 640 MHz sample rate, 0.5 V internal reference, PLL disabled, AIN[1] = −2.0 dBFS, unless otherwise noted.

Table 1.

Parameter	Temp	Min	Typ	Max	Unit
RESOLUTION	Full		16		Bits
ANALOG INPUT BANDWIDTH			10		MHz
ACCURACY					
No Missing Codes	Full		Guaranteed		
Offset Error	Full		±0.025	±0.2	% FSR
Gain Error	Full		±0.7	±2.5	% FSR
Integral Nonlinearity (INL)[2]	25°C		±1.5		LSB
MATCHING CHARACTERISTIC					
Offset Error	Full		±0.035	±0.2	% FSR
Gain Error	Full		±0.2	±1.2	% FSR
TEMPERATURE DRIFT					
Offset Error	Full		±1.5		ppm/°C
Gain Error	Full		±47		ppm/°C
INTERNAL VOLTAGE REFERENCE	Full	496	500	505	mV
ANALOG INPUT					
Input Span, VREF = 0.5 V	Full		2		V p-p diff
Input Resistance	Full		1		kΩ
Input Common Mode	Full	1.7	1.8	1.9	V
POWER SUPPLIES					
Supply Voltage					
AVDD	Full	1.7	1.8	1.9	V
CVDD	Full	1.7	1.8	1.9	V
DVDD	Full	1.7	1.8	1.9	V
DRVDD	Full	1.7	1.8	1.9	V
Supply Current					
I_{AVDD}[2], PLL Enabled	Full		150.7	162	mA
I_{AVDD}[2], PLL Disabled	Full		151.2	161	mA
I_{CVDD}[2], PLL Enabled	Full		57	63	mA
I_{CVDD}[2], PLL Disabled	Full		8	9.2	mA
I_{DVDD}[2]	Full		71.5	78	mA
I_{DRVDD}[2]	Full		0.26	0.3	mA
POWER CONSUMPTION					
Sine Wave Input[2], PLL Disabled	Full		416		mW
Sine Wave Input, PLL Enabled	Full		503		mW
Power-Down Power	25°C		110		mW
Standby Power	25°C		9		mW
Sleep Power	Full		3	4	mW

[1] Input power is referenced to full scale. Therefore, all measurements were taken with a 2 dB signal below full scale, unless otherwise noted.
[2] Measured with a low input frequency, full-scale sine wave with approximately 5 pF loading on each output bit.

AD9267

AC SPECIFICATIONS

All power supplies set to 1.8 V, 640 MHz sample rate, 0.5 V internal reference, PLL disabled, AIN[1] = −2.0 dBFS, unless otherwise noted.

Table 2.

Parameter[2]	Temp	Min	Typ	Max	Unit
SIGNAL-TO-NOISE RATIO (SNR)					
f_{IN} = 2.4 MHz	Full	81	83		dB
f_{IN} = 4.2 MHz	25°C		83		dB
f_{IN} = 8.4 MHz	25°C		83		dB
SPURIOUS-FREE DYNAMIC RANGE (WORST SECOND OR THIRD HARMONIC)[3]					
f_{IN} = 2.4 MHz	Full		−88	−80	dBc
f_{IN} = 4.2 MHz	25°C		−88		dBc
f_{IN} = 8.4 MHz	25°C		<−120		dBc
NOISE SPECTRAL DENSITY					
AIN = −2 dBFS	Full		−155	−153	dBFS/Hz
AIN = −40 dBFS	Full		−156	−155	dBFS/Hz
NOISE FIGURE[2, 4]					
AIN = −2 dBFS	25°C		16		dB
AIN = −40 dBFS	25°C		15		dB
TWO-TONE SFDR					
f_{IN1} = 1.8 MHz @ −8 dBFS, f_{IN2} = 2.1 MHz @ −8 dBFS	25°C		−89.5		dBc
f_{IN1} = 3.7 MHz @ −8 dBFS, f_{IN2} = 4.2 MHz @ −8 dBFS	25°C		−93		dBc
f_{IN1} = 7.2 MHz @ −8 dBFS, f_{IN2} = 8.4 MHz @ −8 dBFS	25°C		−87		dBc
ANALOG INPUT BANDWIDTH	25°C			10	MHz

[1] Input power is referenced to full scale. Therefore, all measurements were taken with a 2 dB signal below full scale, unless otherwise noted.
[2] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions.
[3] Spurious-free dynamic range excluding the second or third harmonic is limited by the FFT size, <−120 dBFS.
[4] Noise figure with respect to 50 Ω. AD9267 internal impedance is 1000 Ω differential. See the AN-835 for a definition.

DIGITAL SPECIFICATIONS

All power supplies set to 1.8 V, 640 MHz sample rate, 2 V p-p differential input, 0.5 V internal reference, PLL disabled, AIN = −2.0 dBFS, unless otherwise noted.

Table 3.

Parameter	Temp	Min	Typ	Max	Unit
DIFFERENTIAL CLOCK INPUTS (CLK+, CLK−)					
Logic Compliance			CMOS[1]/LVDS/LVPECL		
Differential Input Voltage	Full	0.4	0.8	2	V p-p
Input Common-Mode Range	Full		450		mV
High Level Input Current	Full	−60		+60	µA
Low Level Input Current	Full	−60		+60	µA
Input Resistance	Full		20		kΩ diff
Input Capacitance	Full		1		pF
LOGIC INPUTS (SCLK)					
High Level Input Voltage	Full	1.2		DRVDD + 0.3	V
Low Level Input Voltage	Full	0		0.8	V
High Level Input Current	Full	−50		−75	µA
Low Level Input Current	Full	−10		+10	µA
Input Resistance	Full		30		kΩ
Input Capacitance	Full		2		pF
LOGIC INPUTS (SDIO, CSB, RESET)					
High Level Input Voltage	Full	1.2		DRVDD + 0.3	V
Low Level Input Voltage	Full	0		0.8	V
High Level Input Current	Full	−10		+10	µA
Low Level Input Current	Full	+40		+135	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		5		pF
DIGITAL OUTPUTS (D0±x to D3±x)					
ANSI-644					
Logic Compliance			LVDS		
Differential Output Voltage (V_{OD})	Full	247		454	mV
Output Offset Voltage (V_{OS})	Full	1.125		1.375	V
Output Coding (Default)			Twos complement		
Low Power, Reduced Signal Option					
Logic Compliance			LVDS		
Differential Output Voltage (V_{OD})	Full	150		250	mV
Output Offset Voltage (V_{OS})	Full	1.10		1.30	V
Output Coding (Default)			Twos complement		

[1] For voltage swings beyond the specified range, clamping diodes are recommended.

AD9267

SWITCHING SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, unless otherwise noted.

Table 4.

Parameter[1]	Conditions/Comments	Temp	Min	Typ	Max	Unit
CLOCK INPUT PARAMETERS	Using clock multiplier					
Input CLK Rate		Full	30		160	MSPS
CLK± Period		Full	6.25		33.3	ns
CLK± Duty Cycle		Full	40	50	60	%
CLOCK INPUT PARAMETERS	Direct clocking					
Conversion Rate		Full	608	640	672	MSPS
CLK± Period		Full	1.48	1.5625	1.72	ns
CLK± Duty Cycle		Full	40	50	60	%
DATA OUTPUT PARAMETERS						
Data Propagation Delay (t_{PD})[2]		Full	160	510	840	ps
DCO± Propagation Delay (t_{DCO})		Full	-60	268	570	ps
DCO± to Data Skew (t_{SKEW})		Full	180	200	280	Ps
Aperture Uncertainty (Jitter, t_J)		Full		1		ps rms
WAKE-UP TIME						
Power-Down Power		25°C		3		Ms
Standby Power		25°C		9		µs
Sleep Power		25°C		15		µs
OUT-OF-RANGE RECOVERY TIME		25°C		100		ns
SERIAL PORT INTERFACE[3]						
SCLK Period (t_{SCLK})		Full			40	ns
SCLK Pulse Width High Time (t_{SHIGH})		Full	16			ns
SCLK Pulse Width Low Time (t_{SLOW})		Full	16			ns
SDIO to SCLK Set-Up Time (t_{SDS})		Full	5			ns
SDIO to SCLK Hold Time (t_{SDH})		Full	2			ns
CSB to SCLK Set-Up Time (t_{SS})		Full	5			ns
CSB to SCLK Hold Time (t_{SH})		Full	2			ns

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions.
[2] Output propagation delay is measured from CLK± 50% transition to data D0±x to D3±x 50% transition, with 5 pF load.
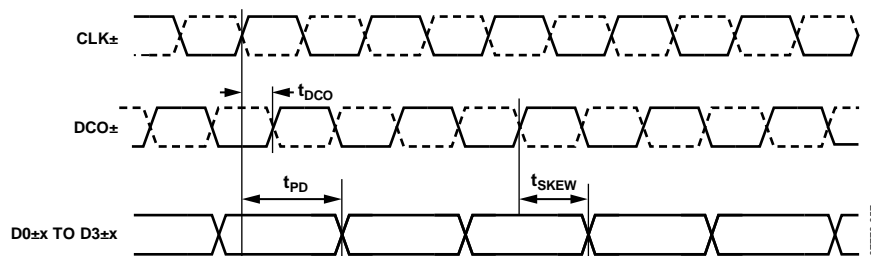[3] See Figure 42 and the Serial Port Interface (SPI) section.

Timing Diagram

Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Electrical	
AVDD to AGND	−0.3 V to +2.0 V
DVDD to DGND	−0.3 V to +2.0 V
DRVDD to DGND	−0.3 V to +3.9 V
AGND to DGND	−0.3 V to +0.3 V
AVDD to DRVDD	−3.9 V to +2.0 V
CVDD to CGND	−0.3 V to +2.0 V
CGND to DGND	−0.3 V to +0.3 V
D0±A to D3±A to DGND	−0.3 V to +2.0 V
D0±B to D3±B to DGND	−0.3 V to +2.0 V
DCO± to DGND	−0.3 V to +2.0 V
OR±A, OR±B to DGND	−0.3 V to +2.0 V
PDWNA to DGND	−0.3 V to +3.9 V
PDWNB to DGND	−0.3 V to +3.9 V
PLLMULTx to DGND	−0.3 V to +3.9 V
SDIO to DGND	−0.3 V to +3.9 V
CSB to AGND	−0.3 V to +3.9 V
SCLK to AGND	−0.3 V to +3.9 V
VIN±A, VIN±B to AGND	−0.3 V to +2.5 V
CLK+, CLK− to CGND	−0.3 V to +2.0 V
Environmental	
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

The exposed paddle must be soldered to the ground plane for the LFCSP package. Soldering the exposed paddle to the PCB increases the reliability of the solder joints, maximizing the thermal capability of the package.

Typical θ_{JA} and θ_{JC} are specified for a 4-layer board in still air. Airflow increases heat dissipation, effectively reducing θ_{JA}. In addition, metal in direct contact with the package leads from metal traces, through holes, ground, and power planes reduces the θ_{JA}.

Table 6. Thermal Resistance

Package Type	θ_{JA}	Unit
64-Lead LFCSP (CP-64-4)	22	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS
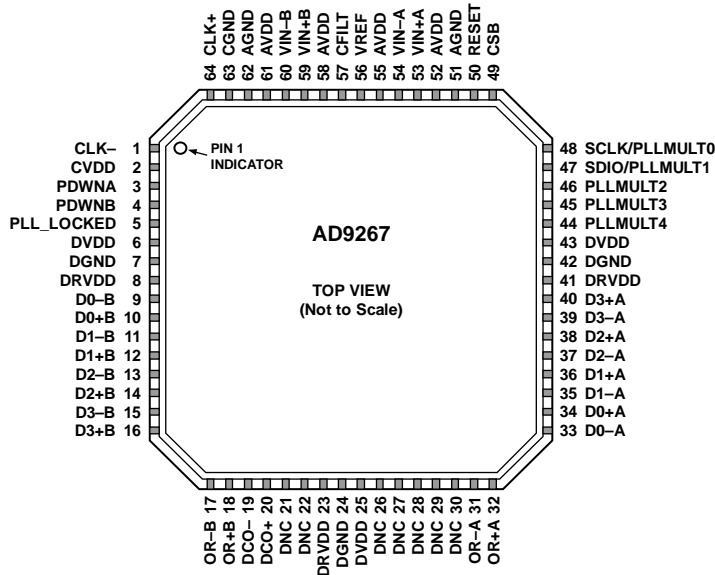
NOTES
1. DNC = DO NOT CONNECT.
2. THE EXPOSED PAD MUST BE SOLDERED TO THE GROUND PLANE FOR THE LFCSP PACKAGE. SOLDERING THE EXPOSED PADDLE TO THE PCB INCREASES THE RELIABILITY OF THE SOLDER JOINTS, MAXIMIZING THE THERMAL CAPACITY OF THE PACKAGE.

Figure 3. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	CLK−	Differential Clock Input (−).
2	CVDD	Clock Supply (1.8 V).
3, 4	PDWNA, PDWNB	Power-Down Pins. Active high.
5	PLL_LOCKED	PLL Lock Indicator.
6, 25, 43	DVDD	Digital Supply (1.8 V).
7, 24, 42	DGND	Digital Ground.
8, 23, 41	DRVDD	Digital Output Driver Supply
9 to 16	D0−B, D0+B to D3−B, D3+B	Channel B Differential LVDS Data Output Bits. D0+B is the LSB and D3+B is the MSB.
17, 18	OR−B, OR+B	Channel B Overrange Indicator Pins.
19, 20	DCO−, DCO+	Differential Data Clock Output.
21, 22, 26 to 30	DNC	Do Not Connect.
31, 32	OR−A, OR+A	Channel A Overrange Indicator Pins.
33 to 40	D0−A, D0+A to D3−A, D3+A	Channel A Differential LVDS Data Output Bits. D0+A is the LSB and D3+A is the MSB.
44, 45, 46	PLLMULT4, PLLMULT3, PLLMULT2	PLL Mode Selection Pins.
47	SDIO/PLLMULT1	Serial Port Interface Data Input/Output/PLL Mode Selection Pins.
48	SCLK/PLLMULT0	Serial Port Interface Clock/PLL Mode Selection Pins.
49	CSB	Serial Port Interface Chip Select Pin Active Low.
50	RESET	Chip Reset.
51, 62	AGND	Analog Ground.
52, 55, 58, 61	AVDD	Analog Supply (1.8 V).
53, 54	VIN+A, VIN−A	Channel A Analog Input.
56	VREF	Voltage Reference Input.
57	CFILT	Noise Limiting Filter Capacitor.
59, 60	VIN+B, VIN−B	Channel B Analog Input.
63	CGND	Clock Ground.
64	CLK+	Differential Clock Input (+).
65	Exposed paddle (EPAD)	Analog Ground. (Pin 65 is the exposed thermal pad on the bottom of the package.) The exposed paddle must be soldered to analog ground of the PCB to achieve optimal electrical and thermal performance.

TYPICAL PERFORMANCE CHARACTERISTICS

All power supplies set to 1.8 V, 640 MHz sample rate, 0.5 V internal reference, PLL disabled, AIN = −2.0 dBFS, T$_A$ = 25°C, unless otherwise noted. The output spectrums shown in Figure 4 through Figure 9 were obtained after 16× decimation at the output of the AD9267 and are shown for a 10 MHz bandwidth.
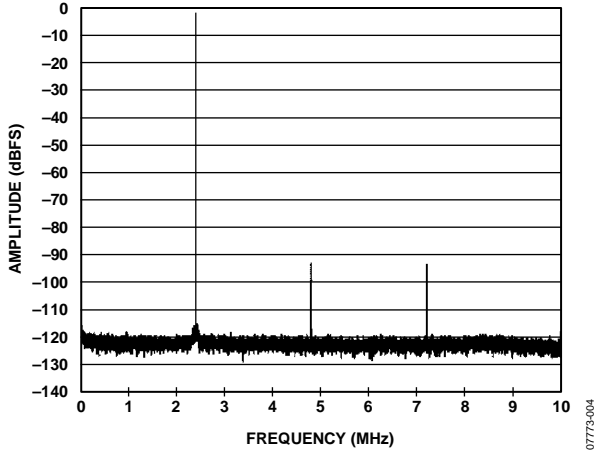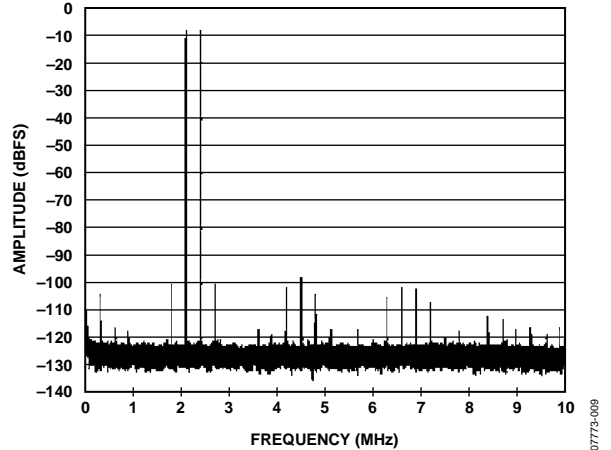

Figure 4. Single-Tone FFT with f$_{IN}$ = 2.4 MHz

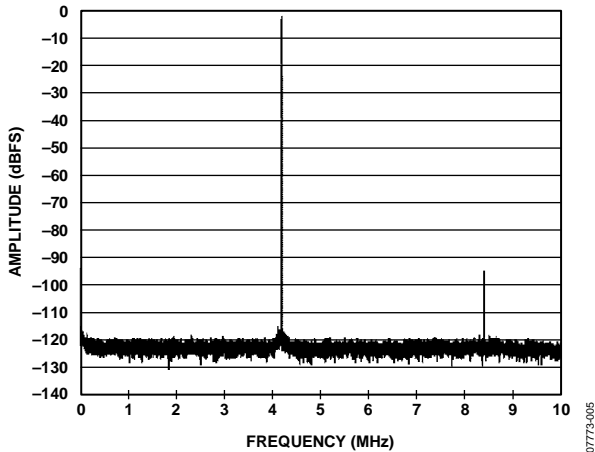*Figure 7. Two-Tone FFT with f$_{IN1}$ = 2.1 MHz, f$_{IN2}$= 2.4 MHz*

Figure 5. Single-Tone FFT with f$_{IN}$ = 4.2 MHz
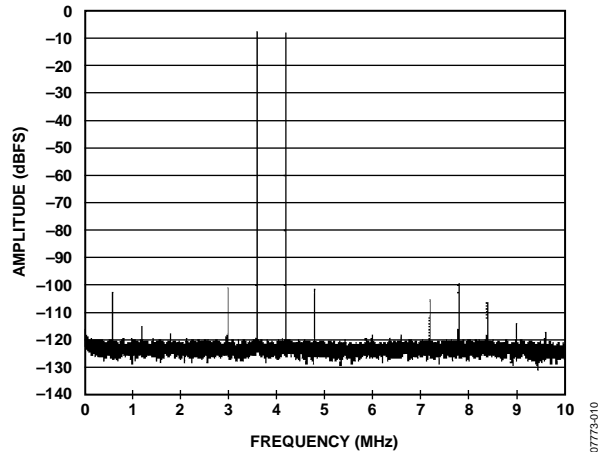
Figure 8. Two-Tone FFT with f$_{IN1}$ = 3.6 MHz, f$_{IN2}$ = 4.2 MHz
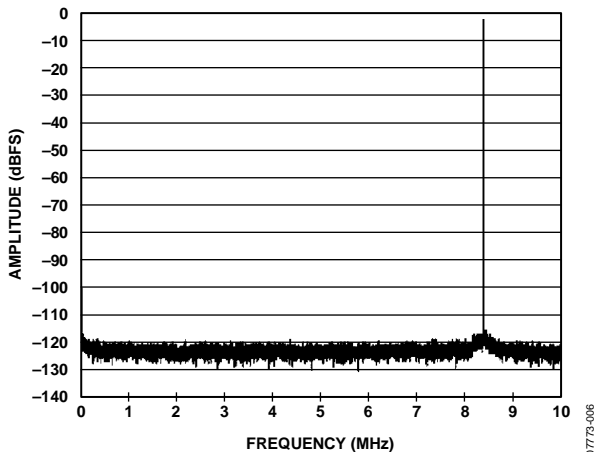
Figure 6. Single-Tone FFT with f$_{IN}$ = 8.4 MHz
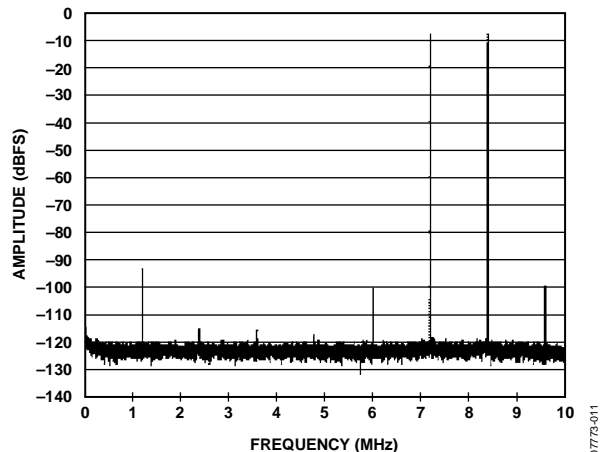
Figure 9. Two-Tone FFT with f$_{IN1}$ = 7.2 MHz, f$_{IN2}$ = 8.4 MHz
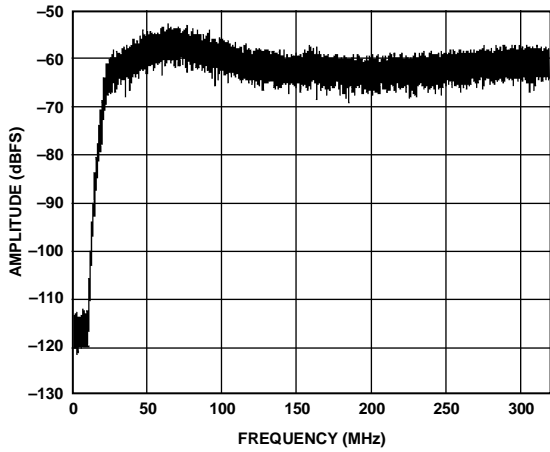
Figure 10. Noise Transfer Function (NTF)

Figure 11. Single-Tone SNR and SFDR vs. Input Amplitude with f_{IN} = 2.4 MHz

Figure 12. SFDR vs. Temperature

Figure 13. Single-Tone SNR vs. Input Frequency

Figure 14. SNR vs. Input Common-Mode Voltage
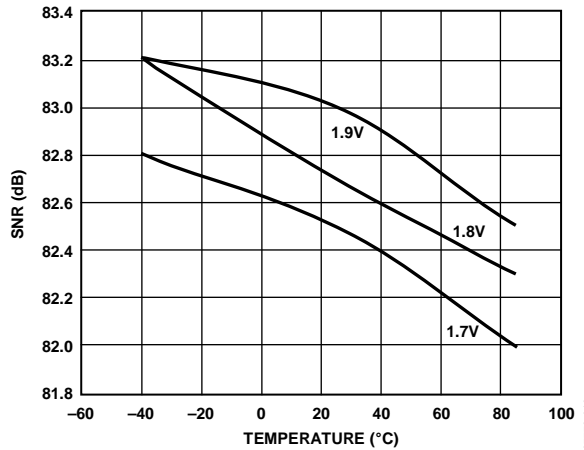

Figure 15. SNR vs. Temperature
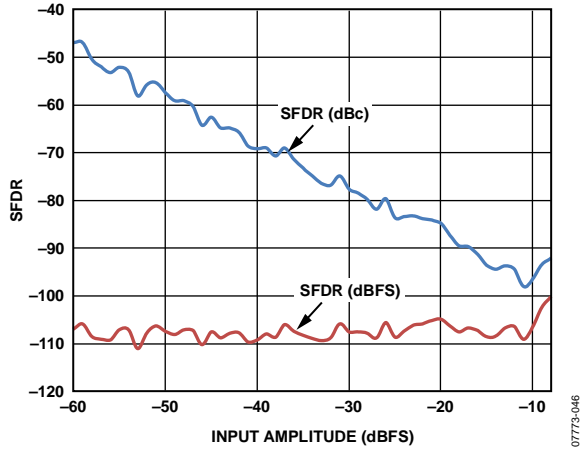
Figure 16. Two-Tone SFDR vs. Input Amplitude with
f_{IN1} = 2.1 MHz, f_{IN2} = 2.4 MHz
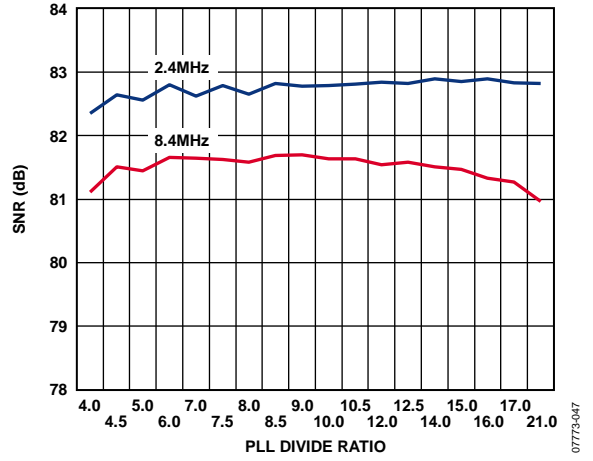

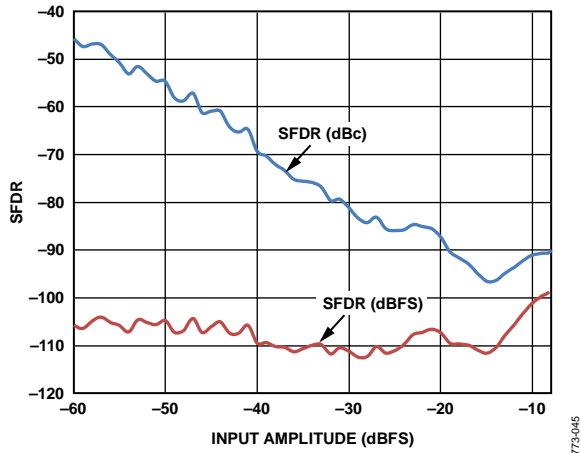Figure 18. Single-Tone SNR vs. PLL Divide Ratio with
f_{IN1} = 2.4 MHz, f_{IN2} = 8.4 MHz

Figure 17. Two-Tone SFDR vs. Input Amplitude with
f_{IN1} = 7.2 MHz, f_{IN2} = 8.4 MHz

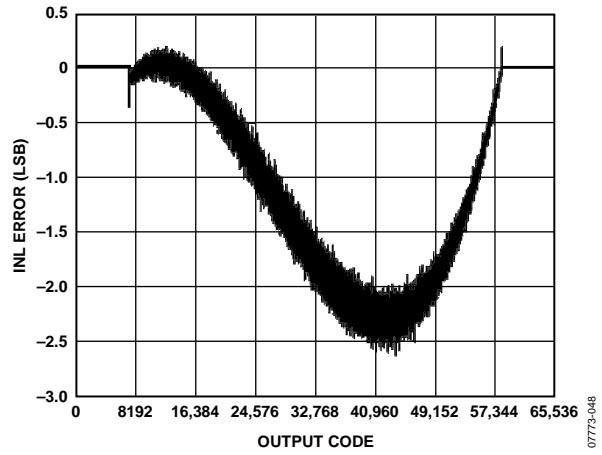Figure 19. INL with f_{IN} = 2.4 MHz

EQUIVALENT CIRCUITS
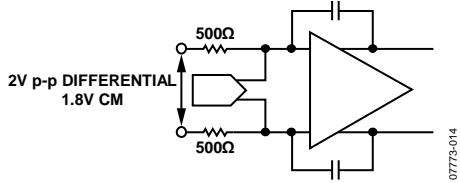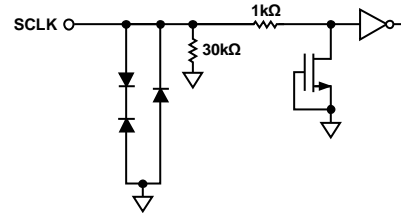

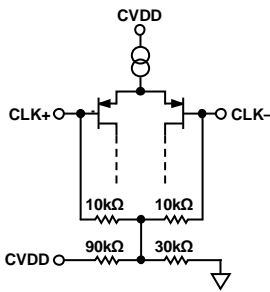Figure 20. Equivalent Analog Input Circuit

Figure 23. Equivalent SCLK Input Circuit

Figure 21. Equivalent Clock Input Circuit
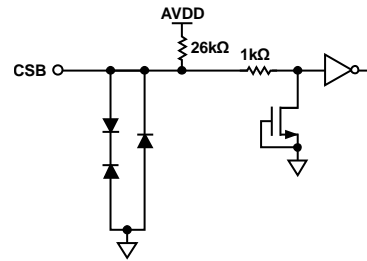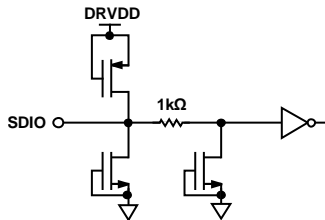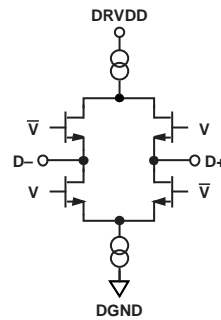

Figure 24. Equivalent CSB Input Circuit

Figure 22. Equivalent SDIO Input Circuit

NOTES
1. D− AND D+ REFERS TO
   THE D0±x TO D3±x PINS.

Figure 25. Equivalent Digital Output Circuit
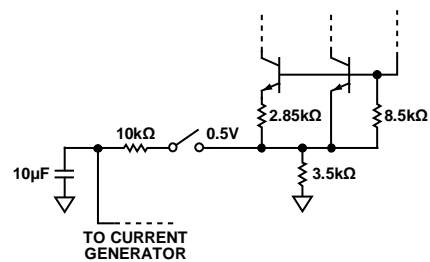

Figure 26. Equivalent VREF Circuit

THEORY OF OPERATION

The AD9267 uses a continuous time Σ-Δ modulator to convert the analog input to a digital word. The modulator consists of a continuous time loop filter preceding a quantizer (see Figure 27), which samples at f_{MOD} = 640 MSPS. This produces an oversampling ratio (OSR) of 32 for a 10 MHz input bandwidth. The output of the quantizer is fed back to a DAC that ideally cancels the input signal. The incomplete input cancellation residue is filtered by the loop filter and is used to form the next quantizer sample.
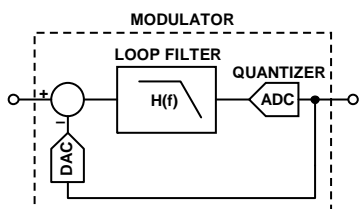

Figure 27. Σ-Δ Modulator Overview

The quantizer produces a nine-level digital word. The quantization noise is spread uniformly over the Nyquist band (see Figure 28) but the feedback loop causes the quantization noise present in the nine-level output to have a nonuniform spectral shape. This noise shaping technique (see Figure 29) pushes the in-band noise out of band; therefore, the amount of quantization noise in the frequency band of interest is minimal.
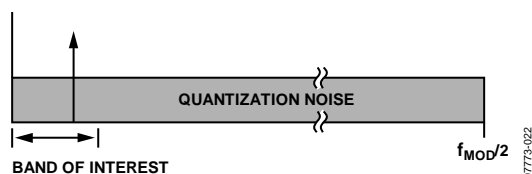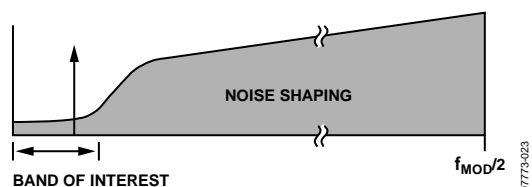

Figure 28. Quantization Noise

Figure 29. Noise Shaping

ANALOG INPUT CONSIDERATIONS

The continuous time modulator removes the need for an anti-alias filter at the input to the AD9267. A discrete time converter aliases signals around the sample clock frequency and its multiples to the band of interest (see Figure 30). An external antialias filter is needed to reject these signals.
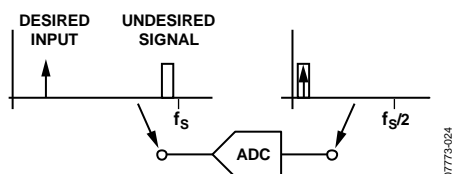
Figure 30. Discrete Time Converter

In contrast, the continuous time Σ-Δ modulator used within the AD9267 has inherent antialiasing. The antialiasing property results from sampling occurring at the output of the loop filter (see Figure 31), and thus aliasing occurs at the same point in the loop as quantization noise is injected; aliases are shaped by the same mechanism as quantization noise. The quantization noise transfer function, NTF(f), has zeros in the band of interest and in all alias bands because NTF(f) is a discrete time transfer function, whereas the loop filter transfer function, LF(f), introduces poles only in the band of interest because LF(f) is a continuous time transfer function. The signal transfer function, being the product of NTF(f) and LF(f), only has zeros in all alias bands and therefore suppresses all aliases.
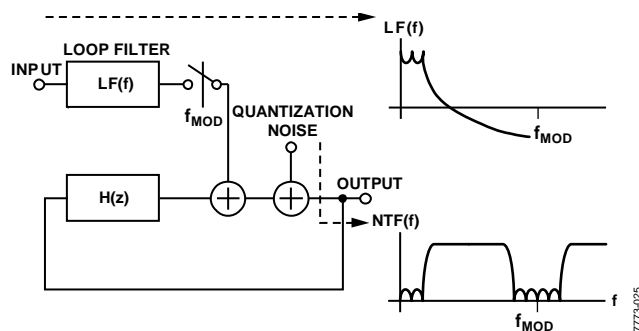
Figure 31. Continuous Time Converter

Input Common Mode

The analog inputs of the AD9267 are not internally dc biased. In ac-coupled applications, the user must provide this bias externally. Setting the device such that V_{CM} = AVDD is recommended for optimum performance. The analog inputs are 500 Ω resistors and the internal reference loop aims to develop 0.5 V across each input resistor (see Figure 32). With 0 V differential input, the driver sources 1 mA into each analog input.
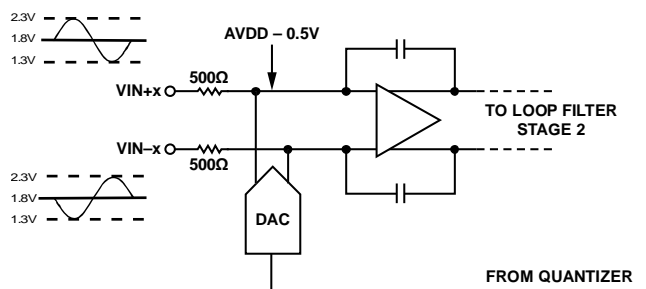
Figure 32. Input Common Mode

AD9267

Differential Input Configurations

Optimum performance can be achieved by driving the AD9267 in a differential input configuration. The ADA4937-2 differential driver provides excellent performance and a flexible interface to the ADC. The output common-mode voltage of the ADA4937-2 is easily set by connecting AVDD to the V_{OCMx} pin of the ADA4937-2 (see Figure 33). The noise and linearity of the ADA4937-2 needs important consideration because the system performance may be limited by the ADA4937-2.
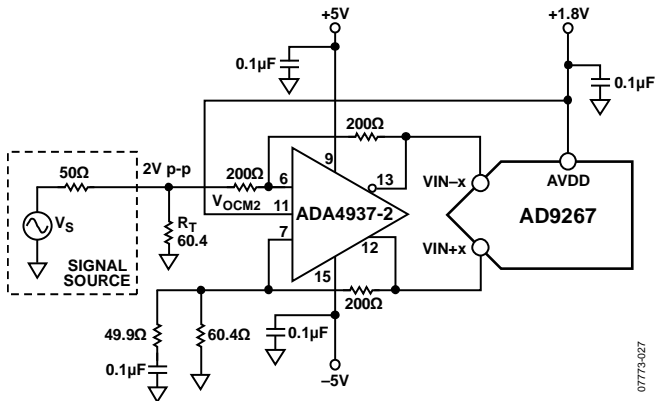
Figure 33. Differential Input Configuration Using the ADA4937-2

For frequencies offset from dc, where SNR is a key parameter, differential transformer coupling is the recommended input configuration. An example is shown in Figure 34. The center tap of the secondary winding of the transformer is connected to AVDD to bias the analog input.

The signal characteristics must be considered when selecting a transformer. Most RF transformers saturate at frequencies below a couple of megahertz (MHz), and excessive signal power can cause core saturation, which leads to distortion.
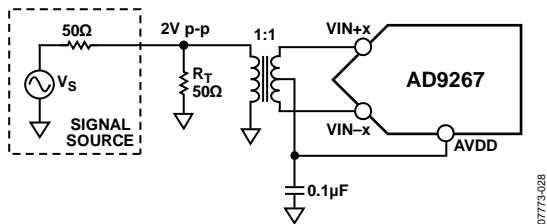
Figure 34. Differential Transformer Configuration

Voltage Reference

A stable and accurate 0.5 V voltage reference is built into the AD9267. The reference voltage should be decoupled to minimize the noise bandwidth using a 10 µF capacitor. The reference is used to generate a bias current into a matched resistor such that when used to bias the current in the feedback DAC, a voltage of AVDD − 0.5 V is developed at the internal side of the input resistors (see Figure 35). The current bias circuit should also be decoupled on the CFILT pin with a 10 µF capacitor. For this reason, the VREF voltage should always be 0.5 V.
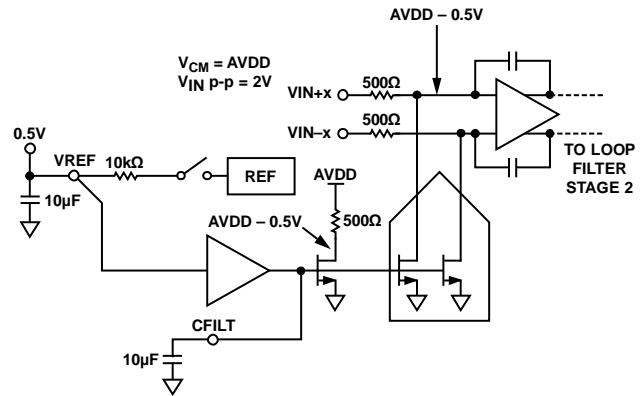
Figure 35. Voltage Reference Loop

Internal Reference Connection

To minimize thermal noise, the internal reference on the AD9267 is an unbuffered 0.5 V. It has an internal 10 kΩ series resistor, which, when externally decoupled with a 10 µF capacitor, limits the noise (see Figure 36). Do not use the unbuffered reference to drive any external circuitry. The internal reference is used by default and when Serial Register 0x18[6] is reset.
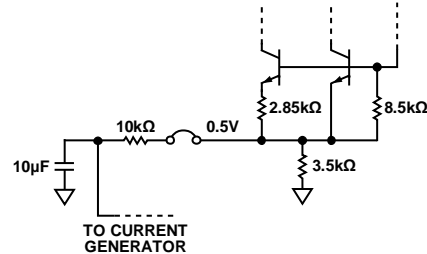
Figure 36. Internal Reference Configuration

External Reference Operation

If an external reference is desired, the internal reference can be disabled by setting Serial Register 0x18[6] high. Figure 37 shows an application using the ADR130B as a stable external reference.
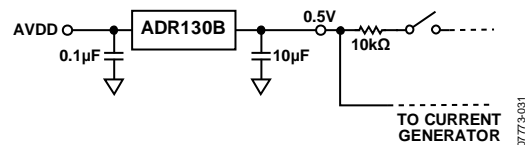
Figure 37. External Reference Configuration

CLOCK INPUT CONSIDERATIONS

The AD9267 offers two modes of sourcing the ADC sample clock (CLK+ and CLK−). The first mode uses an on-chip clock multiplier that accepts a reference clock operating at the lower input frequency. The on-chip phase-locked loop (PLL) then multiplies the reference clock up to a higher frequency, which is then used to generate all the internal clocks required by the Σ-Δ modulator.

The clock multiplier provides a high quality clock that meets the performance requirements of most applications. Using the on-chip clock multiplier removes the burden of generating and distributing the high speed clock.

The second mode bypasses the clock multiplier circuitry and allows the clock to be directly sourced. This mode enables the user to source a very high quality clock directly to the Σ-Δ modulator. Sourcing the clock directly may be necessary in demanding applications that require the lowest possible output noise. Refer to Figure 18, which shows the degradation in SNR performance for the various PLL settings.

In either case, when using the on-chip clock multiplier or sourcing the high speed clock directly, it is necessary that the clock source have low jitter to maximize the Σ-Δ modulator noise performance. High speed, high resolution ADCs and modulators are sensitive to the quality of the clock input. As jitter increases, the SNR performance of the AD9267 degrades from that specified in Table 2. The jitter inherent to the part due to the PLL root sum squares with any external clock jitter, thereby degrading performance. To prevent jitter from dominating the performance of the AD9267, the input clock source should be no greater than 1 ps rms of jitter.

The CLK± inputs are self-biased to 450 mV (see Figure 21); if dc-coupled, it is important to maintain the specified 450 mV input common-mode voltage. Each input pin can safely swing from 200 mV p-p to 1 V p-p single-ended about the 450 mV common-mode voltage. The recommended clock inputs are CMOS or LVPECL.

The specified clock rate of the Σ-Δ modulator, f_{MOD}, is 640 MHz. The clock rate possesses a direct relationship with the available input bandwidth of the ADC.

$$Bandwidth = f_{MOD} \div 64$$

In either case, using the on-chip clock multiplier to generate the Σ-Δ modulator clock rate or directly sourcing the clock, any deviation from 640 MHz results in a change in input bandwidth. The input range of the clock is limited to 640 MHz ± 5%.

Direct Clocking

The default configuration of the AD9267 is for direct clocking where the PLL is bypassed. Figure 38 shows one preferred method for clocking the AD9267. A low jitter clock source is converted from a single-ended signal to a differential signal using an RF transformer. The back-to-back Schottky diodes across the secondary side of the transformer limits clock excursions into the AD9267 to approximately 0.8 V p-p differential. This helps prevent the large voltage swings of the clock from feeding through to other portions of the AD9267 while preserving the fast rise and fall times of the signal, which are critical to achieving low jitter.
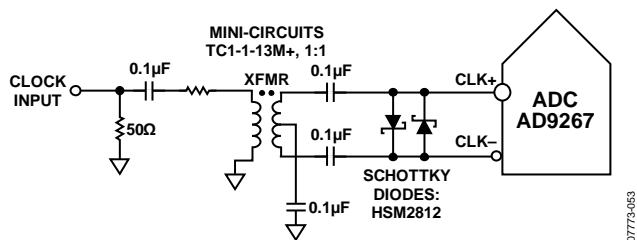
Figure 38. Transformer-Coupled Differential Clock

If a differential clock is not available, the AD9267 can be driven by a single-ended signal into the CLK+ terminal with the CLK− terminal ac-coupled to ground. Figure 39 shows the circuit configuration.
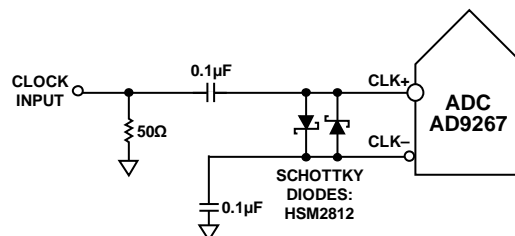
Figure 39. Single-Ended Clock

Another option is to ac couple a differential LVPECL signal to the sample clock input pins, as shown in Figure 40. The AD951x family of clock drivers is recommended because it offers excellent jitter performance.
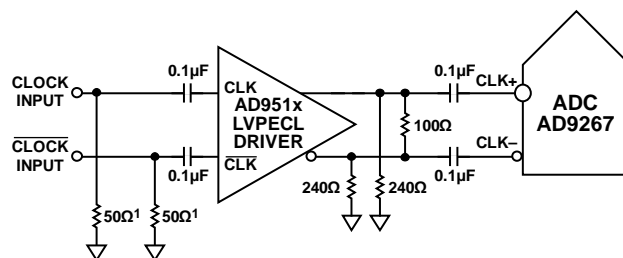
¹50Ω RESISTORS ARE OPTIONAL.

Figure 40. Differential LVPECL Sample Clock

Internal PLL Clock Distribution

The alternative clocking option available on the AD9267 is to apply a low frequency reference clock and use the on-chip clock multiplier to generate the high frequency f_{MOD} rate. The internal clock architecture is shown in Figure 41.
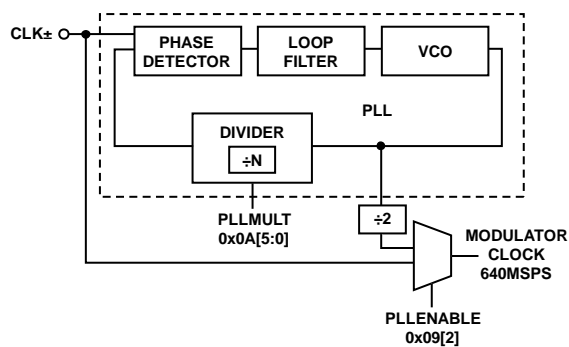
Figure 41. Internal Clock Architecture

The clock multiplication circuit operates such that the VCO outputs a frequency, f_{VCO}, equal to the reference clock input multiplied by N

$$f_{VCO} = (CLK\pm) \times (N)$$

where N is the PLL multiplication (PLLMULT) factor.

The Σ-Δ modulator clock frequency, f_{MOD}, is equal to

$$f_{MOD} = f_{VCO} \div 2$$

The reference clock, CLK±, is limited to 30 MHz to 160 MHz when configured to use the on-chip clock multiplier. Given the input range of the reference clock and the available multiplication factors, the f_{VCO} is approximately 1280 MHz. This results in the desired f_{MOD} rate of 640 MHz with a 50% duty cycle.

The PLL of the AD9267 can be controlled through either the serial port interface or the PLLMULTx pins. For serial port interface control, Register 0x09 and Register 0x0A are used. Before the PLL enable register bit (PLLENABLE) is set, the PLL multiplication factor should be programmed into Register 0x0A[5:0]. After setting the PLLENABLE bit, the PLL locks and reports a locked state in Register 0x0A[7]. If the PLL multiplication factor is changed, the PLL enable bit should be reset and set again. Some common clock multiplication factors are shown in Table 8.

The recommended sequence for enabling and programming the on-chip clock multiplier is as follows:

1. Apply a reference clock to the CLK± pins.
2. Program the PLL multiplication factor in Register 0x0A[5:0]. See Table 8.
3. Enable the PLL; Register 0x09 = 04 (decimal).

External PLL Control

At power-up, the serial interface is disabled until the first serial port access. If the serial interface is disabled, the PLLMULTx pins control the PLL multiplication factor. The five PLLMULTx pins (Pin 44 to Pin 48) offer all the available multiplication factors. If all PLLMULTx pins are tied high, the PLL is disabled and the AD9267 assumes the high frequency modulator clock rate that is applied to the CLK± pins. Table 10 shows the relationship between PLLMULTx pins and the PLL multiplication factor.

PLL Autoband Select

The PLL VCO has a wide operating range that is covered by overlapping frequency bands. For any desired VCO output frequency, there are multiple valid PLL band select values. The AD9267 possesses an automatic PLL band select feature on chip that determines the optimal PLL band setting. This feature can be enabled by writing to Register 0x0A[6] and is the recommended configuration with the PLL clocking option.

Table 8. PLL Multiplication Factors

0x0A[5:0]	PLLMULT (N)	0x0A[5:0]	PLLMULT (N)
1	8	33	32
2	8	34	34
3	8	35	34
4	8	36	34
5	8	37	34
6	8	38	34
7	8	39	34
8	8	40	34
9	9	41	34
10	10	42	42
11	10	43	42
12	12	44	42
13	12	45	42
14	14	46	42
15	15	47	42
16	16	48	42
17	17	49	42
18	18	50	42
19	18	51	42
20	20	52	42
21	21	53	42
22	21	54	42
23	21	55	42
24	24	56	42
25	25	57	42
26	25	58	42
27	25	59	42
28	28	60	42
29	28	61	42
30	30	62	42
31	30	63	42
32	32	64	42

Table 9. Common Modulator Clock Multiplication Factors

CLK± (MHz)	0x0A[5:0] (PLLMULT)	f_{VCO} (MHz)	f_{MOD} (MHz)	BW (MHz)
30.72	42	1290.24	645.12	10.08
39.3216	32	1258.29	629.15	9.83
52.00	25	1300.00	650.00	10.16
61.44	21	1290.24	645.12	10.08
76.80	17	1305.60	652.80	10.20
78.00	17	1326.00	663.00	10.36
78.6432	16	1258.29	629.15	9.83
89.60	15	1344.00	672.00	10.50
92.16	14	1290.24	645.12	10.08
122.88	10	1228.80	614.40	9.60
134.40	10	1344.00	672.00	10.50
153.60	8	1228.80	614.40	9.60
157.2864	8	1258.29	629.15	9.83

Table 10. PLLMULTx Pins and PLL Multiplication Factor

PLLMULT[4:0] Pins	PLL Multiplication Factors (N)
0	8
1	9
2	10
3	12
4	14
5	15
6	16
7	17
8	18
9	20
10	21
11	24
12	25
13	28
14	30
15	32
16	34
17 to 30	42
31	Direct clocking

POWER DISSIPATION AND STANDBY MODE

The AD9267 consumes 415 mW. This power consumption can be further reduced by configuring the chip in channel power-down, standby, or sleep mode. The low power modes turn off internal blocks of the chip including the reference. As a result, the wake-up time is dependent on the amount of circuitry that is turned off. Fewer internal circuits powered down result in proportionally shorter wake-up time. The different low power modes are shown in Table 11. In the standby mode, all clock related activity is disabled in addition to each channel; the references and LVDS outputs remain powered up to ensure a short recovery and link integrity, respectively. During sleep mode, all internal circuits are powered down, putting the device into its lowest power mode; the LVDS outputs are disabled.

Each ADC channel can be independently powered down or both channels can be set simultaneously by writing to the channel index, Register 0x05[1:0]. Additionally, if the serial port interface is not available, each channel can be independently configured by tying the PDWNA (Pin 3) or PDWNB (Pin 4) high.

Table 11. Low Power Modes

Mode	0x08[1:0]	Analog Circuitry	Clock	Ref.
Normal	0x0	On	On	On
Channel Power-Down	0x1	Off	On	On
Standby	0x2	Off	Off	On
Sleep	0x3	Off	Off	Off

DIGITAL OUTPUTS

Digital Output Format

The AD9267 digital bus outputs twos complement, single data rate, LVDS data at 640 MSPS. The output is four bits wide per channel.

The AD9267 supports both the ANSI-644 and a reduced power data format similar to the IEEE1596.3 standard. The default configuration at power-up is ANSI-644. This can be changed to a low power reduced signal option by addressing Register 0x14[7], DRVSTD.

The LVDS driver current is derived on chip and sets the output current at each output equal to a nominal 3.5 mA for the ANSI-644 standard. A 100 Ω differential termination resistor placed at the LVDS receiver inputs result in a nominal 350 mV swing at the receiver. In the reduced power data format, the output swing is limited to 200 mV and the resulting output current into the 100 Ω termination is 2 mA. As a result of the reduced LVDS voltage swing, an additional 25% digital power savings can be achieved over the ANSI-644 standard.

The desired output format can be selected by addressing Register 0x14[7], DRVSTD. The LVDSTERM bits, Register 0x15[5:4], provide either 100 Ω or 200 Ω, or no termination at the output of the data bus. Selecting the appropriate termination resistor is important to allow maximum signal transfer and to minimize reflections for signal integrity. This can be achieved by selecting a termination resistor that impedance matches the termination of the receiver.

Overrange (OR) Condition

An overrange condition can be triggered by large in-band signals that exceed the full-scale range of the Σ-Δ modulator, or it can be triggered by out-of-band signals gained by the transfer characteristics of the modulator. Figure 43 shows the signal transfer function of the Σ-Δ modulator. The modulator output possesses out-of-band gain above 10 MHz. As a result, the input signal may exceed full scale for input frequencies beyond 10 MHz and the ADC may be in an overrange state. The OR±x pins serve as indicators for the overrange condition.

The OR±x pins are synchronous outputs that are updated at the output data rate. The pins indicate whether an overrange condition has occurred within the AD9267. Ideally, OR±x should be latched on the falling edge of DCO± to ensure proper setup-and-hold time. However, because an overrange condition typically extends well beyond one clock cycle (that is, does not toggle at the DCO± rate); data can usually be successfully detected on the rising edge of DCO± or monitored asynchronously. The user has the ability to select how the overrange condition is reported and this is controlled through the SPI bits (AUTORST, OR_IND1, and OR_IND2) in Register 0x111[7:5]. The two modes of operation are normal and data valid mode.

AD9267

In normal operation mode, the analog input can toggle the OR±x pin for a number of clock cycles as it approaches full scale. The OR±x pin is a pulse-width modulated (PWM) signal; therefore, as the analog input increases in amplitude, the duration of OR±x pin toggling increases. Eventually, when the OR±x pin is high for an extended period of time, the ADC overloads; thus, there is little correspondence between analog input and digital output. In this mode, the duration of the OR±x pin can be used as a coarse indicator to the signal amplitude at the input of the ADC. In data valid mode, the OR±x pin remains high when there are no memory access operations taking place, such as internal calibration or factory memory transfer, and the inputs of the ADC are within the operating range.

In either modes of operation, the AUTORST bit can be enabled and this automatically resets the modulator in an overload condition. Because the OR±x signal is a PWM signal and the toggling of OR±x does not always indicate an overload condition, the modulator only resets after 16 consecutive clock cycles where OR±x remains high or if the loop filter becomes saturated. The OR±x pin remains high until the automatic reset has completed.

If the AD9267 is used in a system that incorporates automatic gain control (AGC), the OR±x signals can be used to indicate that the signal amplitude should be reduced. This may be particularly effective for use in maximizing the signal dynamic range if the signal includes high occurrence components that occasionally exceed full scale by a small amount.

TIMING

The AD9267 provides latched data outputs with a latency of seven clock cycles. The AD9267 also provides a data clock output (DCO±) pin intended to assist in capturing the data in an external register. The data outputs are valid on the rising edge of DCO±, unless changed by setting Serial Register 0x16[7] (see the Serial Port Interface (SPI) section). See Figure 2 for a graphical timing description.

Table 12. OR±x Conditions

Reset State	AUTORST	OR_IND1	OR_IND2	Function
Normal Reset Off	0	0	0	If overrange: OR±x = 1, else OR±x = 0
Data Valid Reset Off	0	1	1	If memory access: OR±x = 0, else OR±x = 1
Normal Reset On	1	0	0	If overrange or reset: OR±x = 1, else OR±x = 0
Data Valid Reset On	1	1	1	If memory access, or reset: OR±x = 0, else OR±x = 1

SERIAL PORT INTERFACE (SPI)

The AD9267 serial port interface (SPI) allows the user to configure the converter for specific functions or operations through a structured register space provided inside the ADC. This provides the user added flexibility and customization depending on the application. Addresses are accessed via the serial port and can be written to or read from via the port. Memory is organized into bytes that are further divided into fields, as documented in the Memory Map section. For detailed operational information, see the see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

CONFIGURATION USING THE SPI

As summarized in Table 13, three pins define the SPI of this ADC. The SCLK pin synchronizes the read and write data presented to the ADC. The SDIO pin allows data to be sent and read from the internal ADC memory map registers. The CSB pin is an active low control that enables or disables the read and write cycles.

Table 13. Serial Port Interface Pins

Pin	Function
SCLK	SCLK (serial clock) is the serial shift clock. SCLK synchronizes serial interface reads and writes.
SDIO	SDIO (serial data input/output) is an input and output depending on the instruction being sent and the relative position in the timing frame.
CSB	CSB (chip select) is an active low control that gates the read and write cycles.

The falling edge of CSB in conjunction with the rising edge of the SCLK determines the start of the framing. Figure 42 and Table 14 provide an example of the serial timing and its definitions.

Other modes involving CSB are available. CSB can be held low indefinitely to permanently enable the device (this is called streaming). CSB can stall high between bytes to allow for

additional external timing. When CSB is tied high, SPI functions are placed in a high impedance mode.

During an instruction phase, a 16-bit instruction is transmitted. Data follows the instruction phase and the length is determined by the W0 bit and the W1 bit. All data is composed of 8-bit words. The first bit of each individual byte of serial data indicates whether a read or write command is issued. This allows the serial data input/output (SDIO) pin to change direction from an input to an output.

In addition to word length, the instruction phase determines if the serial frame is a read or write operation, allowing the serial port to be used to both program the chip as well as to read the contents of the on-chip memory. If the instruction is a readback operation, performing a readback causes the serial data input/output (SDIO) pin to change direction from an input to an output at the appropriate point in the serial frame.

Data can be sent in MSB- or in LSB-first mode. MSB first is the default setting on power-up and can be changed via the configuration register. For more information, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

Table 14. SPI Timing Diagram Specifications

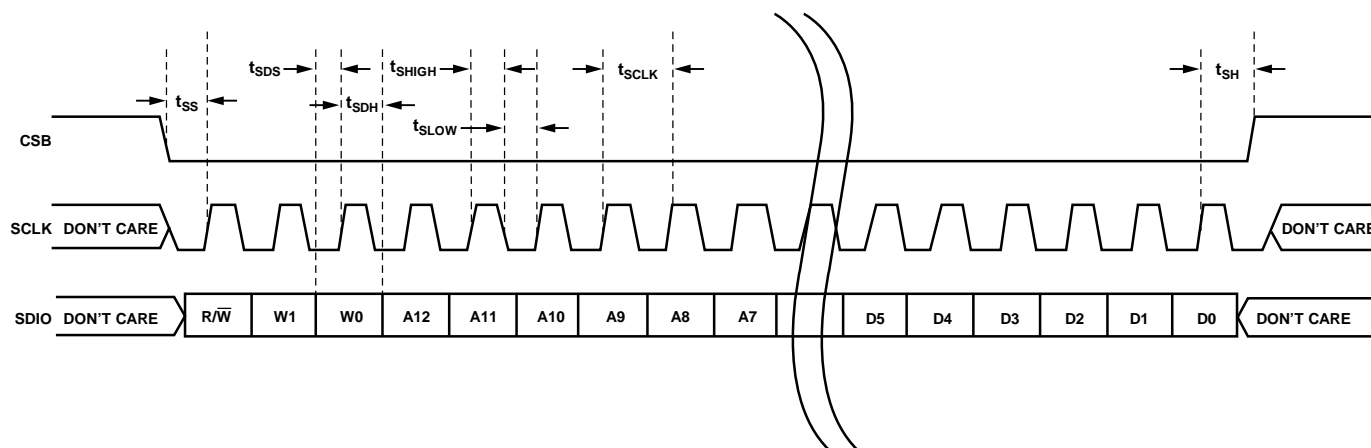| Parameter	Definition
t_{SDS}	Setup time between data and rising edge of SCLK
t_{SDH}	Hold time between data and rising edge of SCLK
t_{SCLK}	Period of the clock
t_{SS}	Setup time between CSB and SCLK
t_{SH}	Hold time between CSB and SCLK
t_{SHIGH}	Minimum period that SCLK should be in a logic high state
t_{SLOW}	Minimum period that SCLK should be in a logic low state

Figure 42. Serial Port Interface Timing Diagram

HARDWARE INTERFACE

The pins described in Table 13 comprise the physical interface between the programming device of the user and the serial port of the AD9267. The SCLK and CSB pins function as inputs when using the SPI interface. The SDIO pin is bidirectional, functioning as an input during write phases and as an output during readback.

The SPI interface is flexible enough to be controlled by either PROM or PIC microcontrollers. This provides the user with the ability to use an alternate method to program the ADC. One such method is described in detail in the AN-812 Application Note, *MicroController-Based Serial Port Interface (SPI) Boot Circuit*.

When the SPI interface is not used, SCLK/PLLMULT0 and SDIO/PLLMULT1 serve a dual function. When strapped to AVDD or ground during device power-on, the pins are associated with a specific function.

APPLICATIONS INFORMATION

FILTERING REQUIREMENT

The need for anti-alias protection often requires one or two octaves for a transition band, which reduces the usable bandwidth of a Nyquist converter to between 25% and 50% of the available bandwidth. A CT Σ-Δ converter maximizes the available signal bandwidth by forgoing the need for an antialiasing filter because the architecture possesses inherent antialiasing. Although a high order, sharp cutoff antialiasing filter may not be necessary because of the unique characteristics of the architecture, a low order filter may still be required to precede the ADC for out-of-band signal handling.

Depending on the application and the system architecture, this low order filter may or may not be necessary. The signal transfer function (STF) of a continuous time feedforward ADC usually contains out-of-band peaks. Because these STF peaks are typically one or two octaves above the pass-band edge, they are not problematic in applications where the bulk of the signal energy is in or near the pass band. However, in applications with large far-out interferers, it is necessary to either add a filter to attenuate these problematic signals or to allocate some of the ADC dynamic range to accommodate them.

Figure 43 shows the normalized STF of the AD9267 CT Σ-Δ converter. The figure shows out-of-band peaking beyond the band edge of the ADC. Within the 10 MHz band of interest, the STF is maximally flat with less than 0.1 dB of gain. Maximum peaking occurs at 60 MHz with 10 dB of gain. To put this into perspective, for a fixed input power, a 5 MHz in-band-signal appears at −5 dBFS, a 25 MHz tone appears at −2 dBFS and 60 MHz tone at +5 dBFS. Because the maximum input to the ADC is −2 dBFS, large out-of-band signals can quickly saturate the system. This implies that under these conditions, the digital outputs of the ADC no longer accurately represents the input. Refer to the Overrange (OR) Condition section for details on overrange detection and recovery.
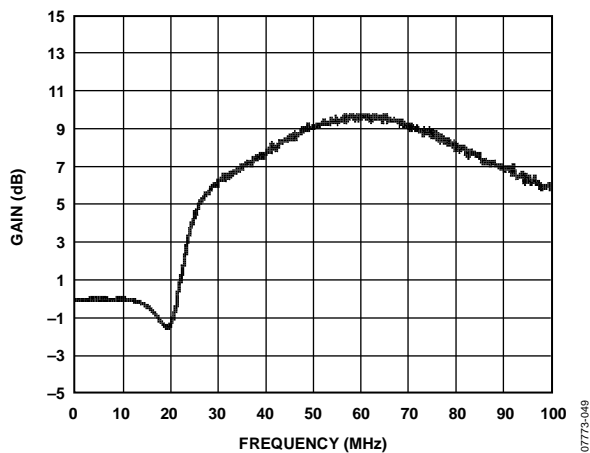

Figure 43. STF

Figure 43 shows the gain profile of the AD9267 and this can be interpreted as the level in which the signal power should be scaled back to prevent an overload condition. This is the ultimate trip point and before this point is reached, the in-band noise (IBN) slowly degrades. As a result, it is recommended that the low-pass filter be designed to match the profile of Figure 44, which shows the maximum input signal for a 3 dB degradation of in-band noise. The input signal is attenuated to allow only 3 dB of noise degradation over frequency.

The noise performance is normalized to a −2 dBFS in-band signal. The AD9267 STF and NTF are flat within the band of interest and should result in almost no change in input level and IBN. Beyond the bandwidth of the AD9267, out-of-band peaking adds gain to the system, therefore requiring the input power to be scaled back to prevent in-band noise degradation. The input power is scaled back to a point where only 3 dB of noise degradation is allowed, therefore resulting in Figure 44.
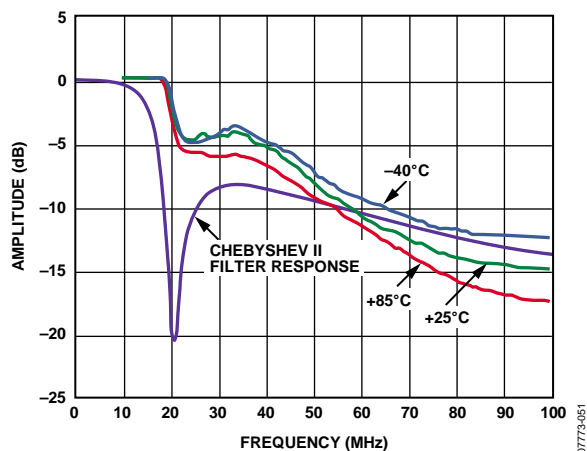

Figure 44. Maximum Input Level for 3 dB Noise Degradation

An example third-order low-pass Chebyshev II type filter is shown in Figure 45 and the corresponding magnitude vs. frequency response of the filter is shown in Figure 44.
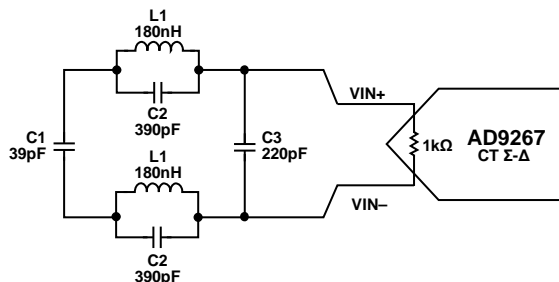

Figure 45. Third-Order Low-Pass Chebyshev II Filter

AD9267

Referring to Figure 46, the 3 dB cutoff frequency of the low-pass Chebyshev II filter response resides at 15.75 MHz, and at 10 MHz, there is 0.43 dB of attenuation due to the sharp roll-off of the filter. Table 15 summarizes the components and manufacturers used to build the circuit.

Table 15. Chebyshev II Filter Components

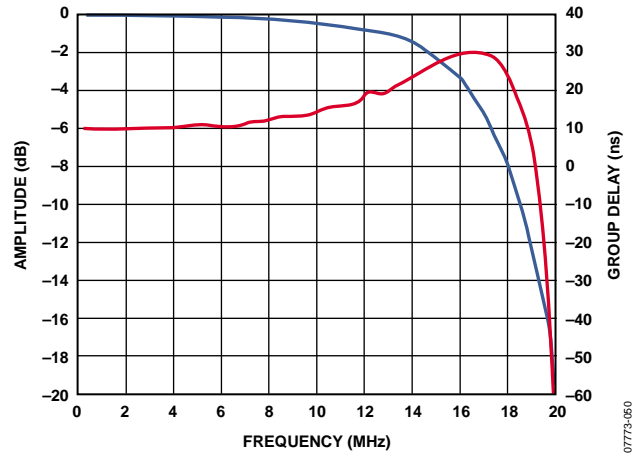| Parameter	Value	Unit	Manufacturer
C1	39	pF	Murata GRM188 series, 0603
L1	180	nH	Coil Craft 0402AF, 2%
C2	390	pF	Murata GRM188 series, 0603
C3	220	pF	Murata GRM188 series, 0603

Figure 46. Low-Pass Chebyshev II Filter Response

In addition to matching the profile of Figure 44, group delay and channel matching are important filter design criteria. Low tolerance components are highly recommended for improved channel matching, which translates to minimal degradation in image rejection for quadrature systems.

MEMORY MAP

Table 16. Memory Map

Register	Address (Hex)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SPI Port Config	00	0	LSBFIRST	SOFTRESET	1	1	SOFTRESET	LSBFIRST	0
Chip ID	01	CHIPID[7:0]							
Chip Grade	02			CHILDID[1:0]					
Channel Index	05							Channel[1:0]	
Power Modes	08							PWRDWN[1:0]	
PLLENABLE	09						PLLENABLE		
PLL	0A	PLLLOCKED	PLLAUTO	PLLMULT[5:0]					
Output Modes	14	DRVSTD			OUTENB				
Output Adjust	15			LVDSTERM[1:0]					
Output Clock	16	DCOINV							
Reference	18		EXTREF						
Overrange	111	AUTORST	OR_IND1	OR_IND2					

MEMORY MAP DEFINITIONS

Table 17. Memory Map Definitions

Register	Address	Bit Name	Bit(s)	Default	Description
SPI Port Config	0x00	LSBFIRST	[6], [1]	0	0: serial interface uses MSB-first format 1: serial interface uses LSB-first format
		SOFTRESET	[5], [2]	0	1: default all serial registers except 0x00, 0x09, and 0x0A
Chip ID	0x01	CHIPID	[7:0]	0x22	0x22: AD9267
Chip Grade	0x02	CHILDID	5:4]	0	0x00: 10 MHz bandwidth 0x10: 5 MHz bandwidth 0x20: 2.5 MHz bandwidth 0x30: modulator only
Channel Index	0x05	Channel	[1:0]	0	0x1: Channel A only addressed 0x2: Channel B only addressed 0x3: both channels addressed simultaneously
Power Modes	0x08	PWRDWN	[1:0]	0	0x0: normal operation 0x1: channel power-down (local) 0x2: standby (everything except reference circuits) 0x3: sleep
PLLENABLE	0x09	PLLENABLE	[2]	0	1: enable PLL
PLL	0x0A	PLLLOCKED	[7]	0	0: PLL is not locked 1: PLL is locked
		PLLAUTO	[6]	0	0: disable PLL auto band select 1: enable PLL auto band select
		PLLMULT	[5:0]	0	See Table 8
Output Modes	0x14	DRVSTD	[7]	0	0: ANSI-644 1: Low power (IEEE1596.3 similar)
		OUTENB	[4]	0	1: Channel A and Channel B outputs tristated
Output Adjust	0x15	LVDSTERM	[5:4]	0	0: no termination 1: 200 Ω 2: 100 Ω 3: 100 Ω
Output Clock	0x16	DCOINV	[7]	0	1: invert DCO±
Reference	0x18	EXTREF	[6]	0	1: use external reference
Overrange	0x111	AUTORST	[7]	0	1: enable autoreset
		OR_IND1	[6]	0	See Table 12
		OR_IND2	[5]	0	See Table 12

OUTLINE DIMENSIONS
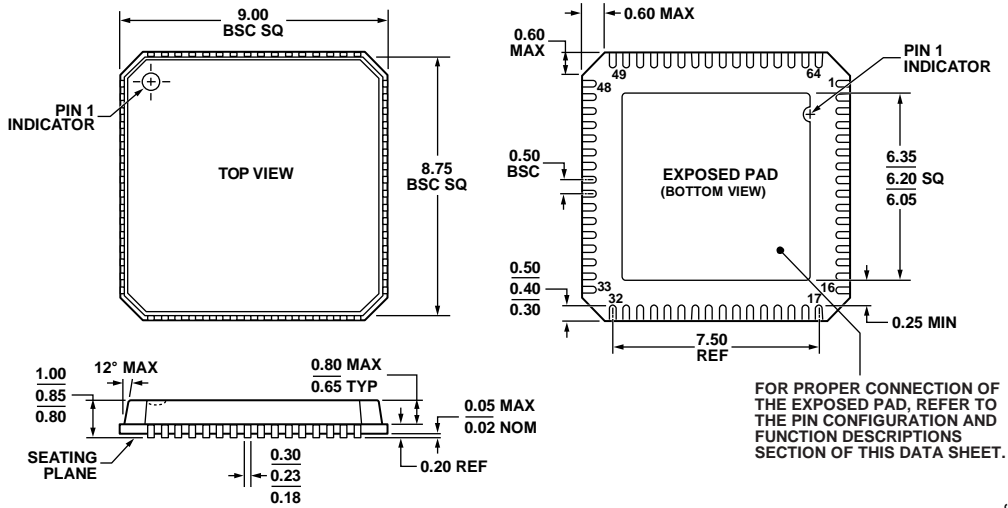
COMPLIANT TO JEDEC STANDARDS MO-220-VMMD-4

Figure 47. 64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
9 mm × 9 mm Body, Very Thin Quad
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9267BCPZ[1]	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-64-4
AD9267EBZ[1]		Evaluation Board	

[1] Z = RoHs Compliant Part.

ANALOG DEVICES

www.analog.com